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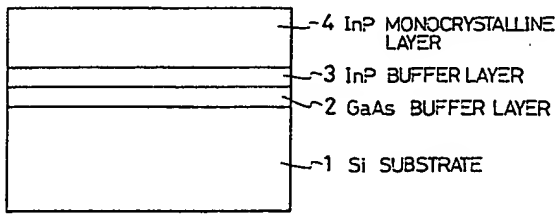
(54) Semiconductor thin film and process for fabricating the same.

(57) An InP semiconductor thin film is formed by a process in which an amorphous GaAs buffer layer (2) having a good surface flatness, and then an amorphous InP buffer layer (3) having a good surface flatness are formed on an Si substrate (1), and then an InP monocrystalline thin film (4) is grown on the InP buffer layer (3). GaAs has a lattice constant intermediate between Si used as the substrate and InP, so the lattice mismatch is reduced.

FIG. 1



EP 0 329 400 A2

Description

SEMICONDUCTOR THIN FILM AND PROCESS FOR FABRICATING THE SAME

The present invention relates to an indium phosphide (InP) semiconductor thin film and process of fabricating the same, and more particularly a process of fabricating a semiconductor thin film comprising an InP monocrystalline layer on an Si substrate used for opto-electronic integrated circuits (OEICs), optical devices, and the like.

In the prior-art process for fabricating an InP semiconductor thin film, an InP monocrystalline thin film is formed directly on an Si substrate.

In another prior-art process, an InP buffer layer is formed on an Si substrate, and then an InP semiconductor thin film is formed on the InP buffer layer.

Figure 2 shows an InP semiconductor thin film formed in the latter process. In the Figure, reference numeral 1 denotes an Si substrate having a surface within a (100) orientation. Reference numeral 3 denotes an InP buffer layer. Reference numeral 4 denotes an InP monocrystalline layer. This InP semiconductor thin film is formed by first using reduced-pressure metal organic chemical vapor deposition (MOCVD), and triethyl-indium (TEI) and phosphine (PH_3) as raw materials, to form the InP buffer layer 3 on the Si substrate 1 at a temperature of 380° C, and then crystal-growing InP monocrystalline thin film 4 on the InP buffer layer 3 at 600° C. As this process achieves InP crystal growth in two steps, this process is called two-step growth method. See for example Ohyobutsuri Gakkai Gakujutsu Koenkai Yokoshu (Preprints of the Symposium of the Japan Society of Applied Physics) 1986 (Autumn), page 706, No. 30p-D-6. The Inp monocrystalline thin film 4 formed by the two- step crystal-growth method has an improved surface state than an InP monocrystalline thin film obtained by the single-step growth method in which an InP monocrystalline film is directly formed on an Si substrate.

However, the surface of the resultant InP semiconductor thin film obtained by the prior-art process is not flat, nor specular (mirror-like), and the film is therefore not satisfactory for practical use. This is considered to be due to the fact that InP having a lattice constant about 8% larger than that of Si is directly crystal-grown on the Si substrate, and crystal defects due to lattice mismatch occur.

An object of the present invention is to eliminate the problem of crystal defects and surface roughness due to the crystal mismatch in the InP semiconductor thin film formed by the prior-art method.

Another object of the present invention is to provide a process of fabricating an InP semiconductor thin film having an InP monocrystalline thin film with an improved crystal quality.

In a process of fabricating an InP semiconductor thin film according to the invention, an Si substrate is heated. an amorphous GaAs buffer layer having a good surface flatness is formed on the Si substrate, then an amorphous InP buffer layer having a good surface flatness is formed on the amorphous GaAs buffer layer, and finally an InP monocrystalline thin film is grown on the InP buffer layer.

The GaAs used for InP semiconductor thin film in the present invention has a lattice constant intermediate between the lattice constants of Si used as the substrate and of InP. Distortion of the lattice of the InP monocrystalline thin film is therefore smaller than if the InP moncrystalline thin film is formed directly on the Si substrate or grown on an InP buffer layer which in turn is formed on an Si substrate.

Incidentally, another method for alleviating lattice mismatch can be contemplated in which a GaAs buffer layer, a GaAs monocrystalline thin film are stacked in this order on an Si substrate. But, according to the invention, the object is accomplished by simply inserting a GaAs layer and without substantially increasing the number of process steps.

In order that the invention may be better understood, some embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings in which:-

Figure 1 is a sectional view for explaining the structure of an InP semiconductor thin film according to the invention;

Figure 2 is a diagram for explaining the structure of a prior-art InP semiconductor thin film; and

Figure 3 is a diagram for showing an example of temperature-time program in the process of the invention.

Figure 1 is a sectional view for explaining an InP semiconductor thin film according to the invention. In the figure, reference numeral 1 denotes an Si substrate having a surface with (100) orientation. Reference numeral 2 denotes a GaAs buffer layer 2. Reference numeral 3 denotes an InP buffer layer. Reference numeral 4 denotes an InP monocrystalline thin film. The InP semiconductor thin film according to the invention has a structure as shown in Figure 1, in which the GaAs buffer layer 2, the InP buffer layer 3, and the InP monocrystalline thin film 4 are stacked in this order on the Si substrate 1.

The Inp semiconductor thin film shown in Figure 1 is fabricated by a process in which the Si substrate 1 is cleaned, the amorphous GaAs buffer layer 2 having a good surface flatness and amorphous InP buffer layer 3 having a good surface flatness are successively formed on the Si substrate 1, and then the InP monocrystalline thin film 4 is grown on the InP buffer layer. The above-mentioned reduced-pressure MOCVD is preferably used for the formation of the layers 2 to 4.

The respective process steps will now be described.

First, a Si substrate is provided. The Si substrate should have a surface with an orientation (100). The amorphous GaAs buffer layer 2 having a good surface flatness is formed on the Si substrate 1. The amorphous GaAs buffer layer 2 having a good

surface flatness can be formed, for example by the method described in the following publication: Journal of Crystal Growth, Vol. 7, Pages 490 to 497 (1986). That is, the Si substrate 1 is first subjected to chemical-etching using hydrofluoric acid (HF) to remove the surface oxide film. Then, the Si substrate 1 is introduced in a reduced-pressure MOCVD reactor. The Si substrate 1 is then subjected to heat-treatment or baking in a mixture gas of arsine (AsH_3) gas and hydrogen and at a temperature of 900°C or higher. With this heat-treatment, the surface of the Si substrate 1 is effectively cleaned. Then, the GaAs buffer layer 2 of a thickness of 200 angstroms or less is formed using arsine gas and trimethyl-gallium (TMG) as raw materials and at a temperature of 450°C or lower (the lower limit is the limit of growth which is about 300°C).

If the GaAs buffer layer 2 is formed under such a condition, an amorphous GaAs buffer layer 2 having a good surface flatness is obtained.

Incidentally, where a GaAs monocrystalline layer is grown directly on the Si substrate 1, there will be lattice mismatch of 4% and the surface will not be flat.

Other conditions of growth can be adopted as long as the GaAs buffer layer 2 is amorphous and has a flat surface.

Next, the amorphous InP buffer layer 3 having a similarly good surface flatness is grown to overlie on the amorphous GaAs buffer layer 2 having a good surface flatness that has thus been grown. The film of the InP buffer layer 3 can be formed using the reduced-pressure MOCVD, at a temperature or 550°C or lower (the lower limit is the limit of growth which is about 300 to 350°C), and using phosphine and trimethyl-indium (TMI) or triethyl-indium (TEI) as raw materials, with a molar ratio PH_3/TMI or TEI being in the order of 500. The InP buffer layer 3 will be an amorphous film having a good surface flatness. It is more desirable that the InP buffer layer 3 is thinner, within the limit in which the lattice distortion can be alleviated. The thickness of about 200 angstroms is preferable.

On top of the InP buffer layer 3, the InP monocrystalline thin film 4 is grown to a predetermined thickness, at a temperature of 600 to 650°C. As the raw materials, phosphine and TMI or TEI can be used with the molar ratio PH_3/TMI or TEI being about 100.

Figure 3 shows an example of temperature-time program in the present invention. The exact time in the figure differs depending on the growth conditions, and should be determined to give the predetermined film thickness.

In the present invention, both of the GaAs buffer layer 2 and the InP buffer layer 3 are formed at a temperature lower, by 100 to 200°C or more, than the normal crystal growth temperature. Accordingly, flat layers are obtained even on a crystal having a substantially different lattice constant. However, these layers have poor monocrystalline quality, as evidenced by X-ray diffraction, or the like, and cannot be used for formation of semiconductor devices. For this reason, InP having a good monocrystalline quality is grown at a temperature of 600° or higher.

It is considered that the GaAs buffer layer 2 and the InP buffer layer 3 having poor crystal quality serve to alleviate distortion in the lattice within InP monocrystalline layer during temperature elevation above 600°C or during growth of the InP monocrystalline thin film 4, and while many crystal defects are left in these buffer layers, the InP monocrystalline thin film 4 will have a good flatness and good crystal quality.

As has been described in detail, a GaAs buffer layer having a lattice constant intermediate between the InP and Si is formed on the Si substrate, and InP buffer layer is formed thereon, to form two-layer buffer layer. Accordingly, distortion and crystal defects due to lattice mismatch can be absorbed, and their occurrence can thereby be avoided. As a result, on the buffer layer, an InP monocrystalline thin film having a flat surface and a good crystal quality can be formed.

Claims

1. An InP semiconductor thin film comprising:
an Si substrate;
a GaAs buffer layer formed on the Si substrate;
an InP buffer layer formed on the GaAs buffer layer; and
an InP monocrystalline thin film formed on the GaAs buffer layer.

2. An InP semiconductor thin film according to Claim 1, wherein said Si substrate has a surface with substantially (100) orientation.

3. An InP semiconductor thin film according to Claim 1, wherein said GaAs buffer layer is an amorphous GaAs layer.

4. An InP semiconductor thin film according to Claim 1, wherein said InP buffer layer is an amorphous InP layer.

5. A process for fabricating an InP semiconductor thin film, comprising the steps of;
providing an Si substrate;
performing heat-treatment of the Si substrate;
forming an amorphous GaAs buffer layer having a good surface flatness on the Si substrate;
forming an amorphous InP buffer layer having a good surface flatness on the GaAs buffer layer; and
growing an InP monocrystalline thin film on the InP buffer layer.

6. A process according to Claim 5, wherein said Si substrate has a surface with substantially (100) orientation.

7. A process according to Claim 5, further comprising the step of performing chemical-etching of the surface of the Si substrate using hydrofluoric acid to remove surface oxide film on the Si substrate;
wherein said heat-heat treatment is performed in a mixture gas of arsine gas (AsH_3) and hydrogen and at a temperature of 900°C or higher.

8. A process according to Claim 7, wherein said heat-treatment is performed in a reduced-

pressure MOCVD reactor in which the subsequent formation of the GaAs buffer layer and the InP buffer layer performed.

9. A process according to Claim 5, wherein said GaAs buffer layer is formed to a thickness of about 200 angstroms or less by a reduced-pressure metal organic chemical vapor deposition using arsine gas and trimethyl-gallium (TMG) as raw materials and at a temperature of 450° C or lower (the lower limit is the limit of growth which is about 300° C).

10. A process according to Claim 5, wherein said InP buffer layer is formed by a reduced-pressure metal organic chemical vapor deposition at a temperature of 550° C or lower, and using phosphine and trimethyl-indium (TMI) or triethyl-indium (TEI) as raw materials, with a molar ratio PH_3/TMI or TEI being in the order of 500.

11. A process according to Claim 10, wherein said reduced-pressure metal organic chemical vapor deposition is performed at a temperature not lower than about 300° C.

12. A process according to Claim 10, wherein the thickness of the InP buffer layer is the thinnest within the limit in which the lattice distortion can be alleviated.

13. A process according to Claim 12, wherein the thickness of the InP buffer layer is about 200 angstroms.

14. A process according to Claim 5, wherein said InP monocrystalline thin film is grown to a predetermined thickness, at a temperature of 600 to 650° C, using phosphine and TMI or TEI, as raw materials, with the molar ratio PH_3/TMI or TEI being about 100.

FIG. 1

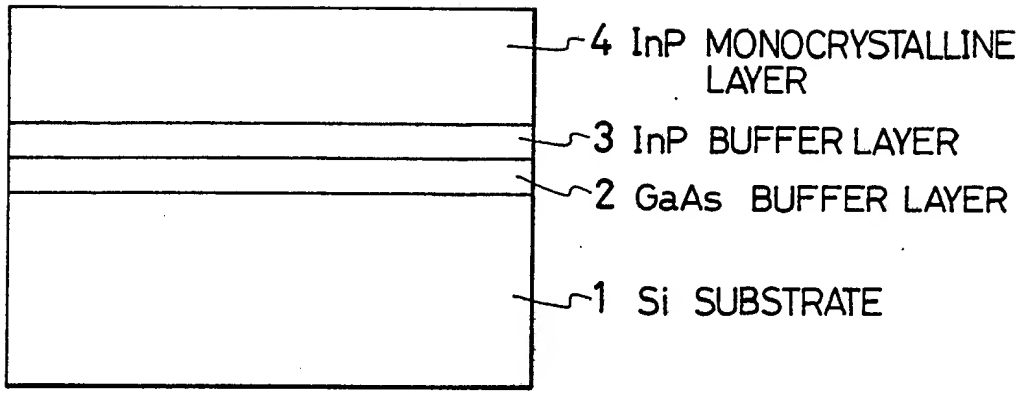

4 InP MONOCRYSTALLINE LAYER
3 InP BUFFER LAYER
2 GaAs BUFFER LAYER
1 Si SUBSTRATE

FIG. 2

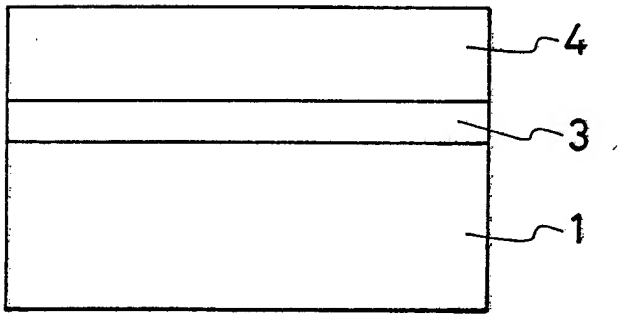

4
3
1

FIG.3

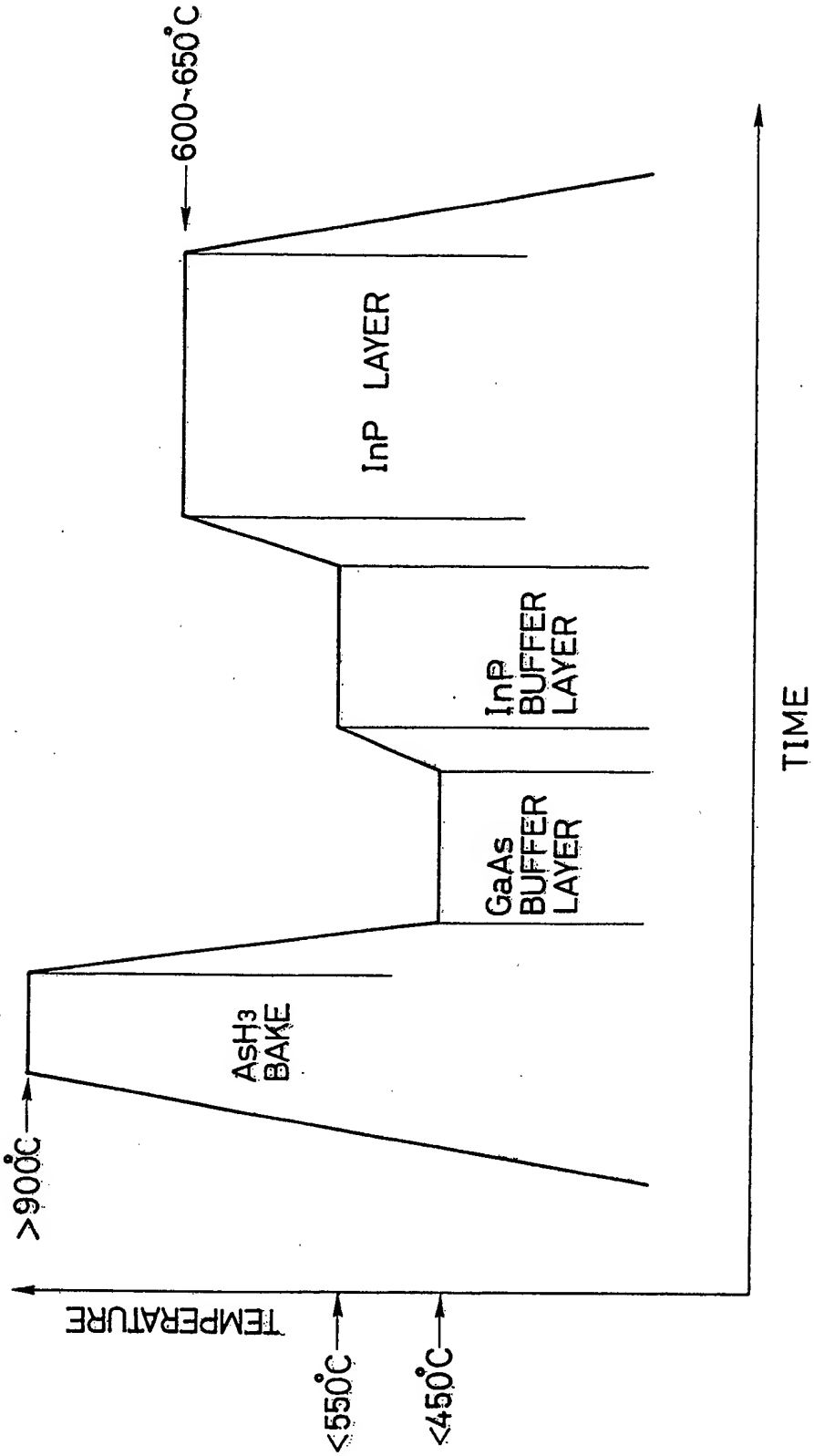

600~650°C
InP LAYER
InP BUFFER LAYER
GaAs BUFFER LAYER
AsH3 BAKE
>900°C
TEMPERATURE
<550°C
<450°C
TIME

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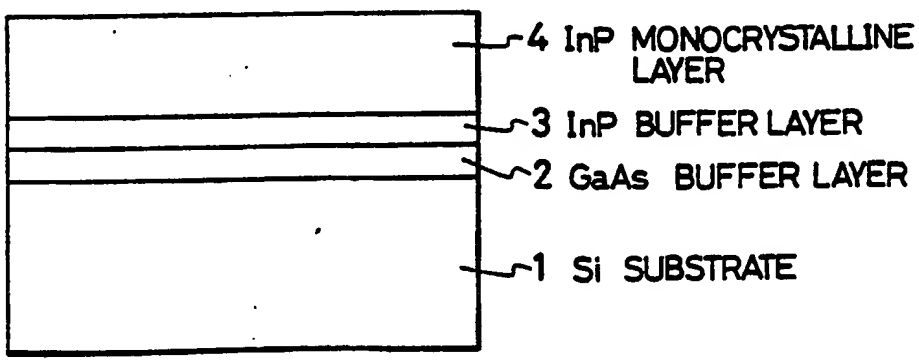
FIG. 1



EP 0 329 400 A3

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 89 30 1423

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
X	US-A-4561916 (M.AKIYAMA ET AL.) * the whole document *	1, 2	H01L31/18 H01L33/00
A	* the whole document *	5-13	H01L21/205
A	SOLID STATE TECHNOLOGY. vol. 30, no. 11, November 1987, WASHINGTON US pages 91 - 97; K.KAMINISHI: "GaAs ON Si TECHNOLOGY" * page 91, right-hand column, line 1 - page 93, right-hand column, line 35 *	1, 2, 5-9	
A	APPLIED PHYSICS LETTERS. vol. 52, no. 3, 18 January 1988, NEW YORK US pages 209 - 211; M.Razeghi et al.: "High-quality GaInAsP/InP heterostructures grown by low-pressure metalorganic chemical vapor deposition on silicon substrates" * the whole document *	1, 8, 9, 10	
X,P	EP-A-291346 (SHARP KABUSHIKI KAISHA) * page 6, line 15 - page 7, line 28; figure 3 *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.4)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	14 JUNE 1990	LINA F.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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(56) References cited:
EP-A- 0 291 346
US-A- 4 561 916

SOLID STATE TECHNOLOGY. vol. 30, no. 11, November 1987, WASHINGTON US pages 91 - 97; K.KAMINISHI: "GaAs ON SI TECHNOLOGY"

APPLIED PHYSICS LETTERS. vol. 52, no. 3, 18 January 1988, NEW YORK US pages 209 - 211; M.Razeghi et al.: "High-quality GaInAsP/InP heterostructures grown by low-pressure metalorganic chemical vapor deposition on silicon substrates"

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Description

The present invention relates to an indium phosphide (InP) semiconductor thin film and process of fabricating the same, and more particularly a process of fabricating a semiconductor thin film comprising an InP monocrystalline layer on an Si substrate used for opto-electronic integrated circuits (OEICs), optical devices, and the like.

In the prior-art process for fabricating an InP semiconductor thin film, an InP monocrystalline thin film is formed directly on an Si substrate.

In another prior-art process, an InP buffer layer is formed on an Si substrate, and then an InP semiconductor thin film is formed on the InP buffer layer.

Figure 2 shows an InP semiconductor thin film formed in the latter process. In the Figure, reference numeral 1 denotes an Si substrate having a surface within a (100) orientation. Reference numeral 3 denotes an InP buffer layer. Reference numeral 4 denotes an InP monocrystalline layer. This InP semiconductor thin film is formed by first using reduced-pressure metal organic chemical vapor deposition (MOCVD), and triethyl-indium (TEI) and phosphine (PH_3) as raw materials, to form the InP buffer layer 3 on the Si substrate 1 at a temperature of 380°C, and then crystal-growing InP monocrystalline thin film 4 on the InP buffer layer 3 at 600°C. As this process achieves InP crystal growth in two steps, this process is called two-step growth method. See for example Ohyobutsuri Gakkai Gakujutsu Koenkai Yokoshu - (Preprints of the Symposium of the Japan Society of Applied Physics) 1986 (Autumn), page 706, No. 30p-D-6. The Inp monocrystalline thin film 4 formed by the two-step crystal-growth method has an improved surface state than an InP monocrystalline thin film obtained by the single-step growth method in which an InP monocrystalline film is directly formed on an Si substrate.

However, the surface of the resultant InP semiconductor thin film obtained by the prior-art process is not flat, nor specular (mirror-like), and the film is therefore not satisfactory for practical use. This is considered to be due to the fact that InP having a lattice constant about 8% larger than that of Si is directly crystal-grown on the Si substrate, and crystal defects due to lattice mismatch occur.

In EP-A-0291346 which belongs to the state of the art according to Article 54(3) EPC there is described a laminated semiconductor structure comprising an Si substrate, a compound GaAs layer composed of a GaAs layer formed at low temperature and a GaAs layer formed at high temperature, a compound InP layer composed of an InP layer formed at low temperature and an InP layer formed at high temperature, a compound semiconductor layer composed of a plurality of alternate layers consisting of $InAsxP_{1-x}$ ($0 < x < 1$) thin layers and InP thin layers and a compound InP layer, in that order.

In US-A-4561916 there is described a method of forming a compound semiconductor comprising an Si substrate on which is formed a layer of a Group III-V compound semiconductor and on which in turn is formed a compound layer comprising alternating layers of: (1) the same Group III-V compound semiconductor as in the first-mentioned layer and (2) a Group III-V compound semiconductor having a lattice constant approximating that of the compound semiconductor in the first alternate layer. Finally a layer of a desired Group III-V compound semiconductor is grown on the alternating layers.

The present invention seeks to eliminate the problem of crystal defects and surface roughness due to the crystal mismatch in the InP semiconductor thin film formed by the prior-art method.

The present invention also seeks to provide a process of fabricating an InP semiconductor thin film having an InP monocrystalline thin film with an improved crystal quality.

According to a first aspect of the invention, there is provided an InP semiconductor thin film comprising:

an Si substrate;

an amporphous GaAs buffer layer formed on the Si substrate;

an amporphous InP buffer layer formed on the GaAs buffer layer; and

an InP monocrystalline thin film formed on the InP buffer layer.

According to a second aspect of the invention, there is provided a process for fabricating an InP semiconductor thin film, said process comprising the steps of;

providing an Si substrate;

performing heat-treatment of the Si substrate;

forming an amorphous GaAs buffer layer having a good surface flatness on the Si substrate;

forming an amorphous InP buffer layer having a good surface flatness on the GaAs buffer layer; and

growing an InP monocrystalline thin film on the InP buffer layer.

The GaAs used for InP semiconductor thin film in the present invention has a lattice constant intermediate between the lattice constants of Si used as the substrate and of InP. Distortion of the lattice of the InP monocrystalline thin film is therefore smaller than if the InP moncrystalline thin film is formed directly on the Si substrate or grown on an InP buffer layer which in turn is formed on an Si substrate.

Incidentally, another method for alleviating lattice mismatch can be contemplated in which a GaAs buffer layer, a GaAs monocrystalline thin film are stacked in this order on an Si substrate. But, according to the invention, the object is accomplished by simply inserting a GaAs layer and without substantially increasing the number of process steps.

In order that the invention may be better understood, some embodiments of the invention will now be described by way of example only and with reference to the accompanying drawings in which:-

Figure 1 is a sectional view for explaining the structure of an InP semiconductor thin film according to the invention;

Figure 2 is a diagram for explaining the structure of a prior-art InP semiconductor thin film; and

Figure 3 is a diagram for showing an example of temperature-time program in the process of the invention.

Figure 1 is a sectional view for explaining an InP semiconductor thin film according to the invention. In the figure, reference numeral 1 denotes an Si substrate having a surface with (100) orientation. Reference numeral 2 denotes a GaAs buffer layer 2. Reference numeral 3 denotes an InP buffer layer. Reference numeral 4 denotes an InP monocrystalline thin film. The InP semiconductor thin film according to the invention has a structure as shown in Figure 1, in which the GaAs buffer layer 2, the InP buffer layer 3, and the InP monocrystalline thin film 4 are stacked in this order on the Si substrate 1.

The InP semiconductor thin film shown in Figure 1 is fabricated by a process in which the Si substrate 1 is cleaned, the amorphous GaAs buffer layer 2 having a good surface flatness and amorphous InP buffer layer 3 having a good surface flatness are successively formed on the Si substrate 1, and then the InP monocrystalline thin film 4 is grown on the InP buffer layer. The above-mentioned reduced-pressure MOCVD is preferably used for the formation of the layers 2 to 4.

The respective process steps will now be described.

First, a Si substrate is provided. The Si substrate should have a surface with an orientation (100). The amorphous GaAs buffer layer 2 having a good surface flatness is formed on the Si substrate 1. The amorphous GaAs buffer layer 2 having a good surface flatness can be formed, for example by the method described in the following publication: Journal of Crystal Growth, Vol. 7, Pages 490 to 497 (1986). That is, the Si substrate 1 is first subjected to chemical-etching using hydrofluoric acid (HF) to remove the surface oxide film. Then, the Si substrate 1 is introduced in a reduced-pressure MOCVD reactor. The Si substrate 1 is then subjected to heat-treatment or baking in a mixture gas of arsine (AsH_3) gas and hydrogen and at a temperature of 900 °C or higher. With this heat-treatment, the surface of the Si substrate 1 is effectively cleaned. Then, the GaAs buffer layer 2 of a thickness of 20 nm (200 angstroms) or less is formed using arsine gas and trimethyl-gallium (TMG) as raw materials and at a temperature of 450 °C or lower (the lower limit is the limit of growth which is about 300 °C).

If the GaAs buffer layer 2 is formed under such a condition, an amorphous GaAs buffer layer 2 having a good surface flatness is obtained.

Incidentally, where a GaAs monocrystalline layer is grown directly on the Si substrate 1, there will be lattice mismatch of 4% and the surface will not be flat.

Other conditions of growth can be adopted as long as the GaAs buffer layer 2 is amorphous and has a flat surface.

Next, the amorphous InP buffer layer 3 having a similarly good surface flatness is grown to overlie on the amorphous GaAs buffer layer 2 having a good surface flatness that has thus been grown. The film of the InP buffer layer 3 can be formed using the reduced-pressure MOCVD, at a temperature of 550 °C or lower (the lower limit is the limit of growth which is about 300 to 350 °C), and using phosphine and trimethyl-indium (TMI) or triethyl-indium (TEI) as raw materials, with a molar ratio PH_3/TMI or TEI being in the order of 500. The InP buffer layer 3 will be an amorphous film having a good surface flatness. It is more desirable that the InP buffer layer 3 is thinner, within the limit in which the lattice distortion can be alleviated. The thickness of about 20 nm (200 angstroms) is preferable.

On top of the InP buffer layer 3, the InP monocrystalline thin film 4 is grown to a predetermined thickness, at a temperature of 600 to 650 °C. As the raw materials, phosphine and TMI or TEI can be used with the molar ratio PH_3/TMI or TEI being about 100.

Figure 3 shows an example of temperature-time program in the present invention. The exact time in the figure differs depending on the growth conditions, and should be determined to give the predetermined film thickness.

In the present invention, both of the GaAs buffer layer 2 and the InP buffer layer 3 are formed at a temperature lower, by 100 to 200 °C or more, than the normal crystal growth temperature. Accordingly, flat layers are obtained even on a crystal having a substantially different lattice constant. However, these layers have poor monocrystalline quality, as evidenced by X-ray diffraction, or the like, and cannot be used for formation of semicon-

ductor devices. For this reason, InP having a good monocrystalline quality is grown at a temperature of 600 ° or higher.

It is considered that the GaAs buffer layer 2 and the InP buffer layer 3 having poor crystal quality serve to alleviate distortion in the lattice within InP monocrystalline layer during temperature elevation above 600 ° C or during growth of the InP monocrystalline thin film 4, and while many crystal defects are left in these buffer layers, the InP monocrystalline thin film 4 will have a good flatness and good crystal quality.

As has been described in detail, a GaAs buffer layer having a lattice constant intermediate between the InP and Si is formed on the Si substrate, and InP buffer layer is formed thereon, to form two-layer buffer layer. Accordingly, distortion and crystal defects due to lattice mismatch can be absorbed, and their occurrence can thereby be avoided. As a result, on the buffer layer, an InP monocrystalline thin film having a flat surface and a good crystal quality can be formed.

Claims

1. An InP semiconductor thin film comprising:
   an Si substrate (1);
   an amporphous GaAs buffer layer (2) formed on the Si substrate;
   an amporphous InP buffer layer (3) formed on the GaAs buffer layer (2); and
   an InP monocrystalline thin film (4) formed on the InP buffer layer (3).

2. An InP semiconductor thin film according to Claim 1, wherein said Si substrate (1) has a surface with substantially (100) orientation.

3. A process for fabricating an InP semiconductor thin film, said process comprising the steps of;
   providing an Si substrate (1);
   performing heat-treatment of the Si substrate (1);
   forming an amorphous GaAs buffer layer (2) having a good surface flatness on the Si substrate (1);
   forming an amorphous InP buffer layer (3) having a good surface flatness on the GaAs buffer layer; and
   growing an InP monocrystalline thin film (4) on the InP buffer layer (3).

4. A process according to Claim 3, wherein said Si substrate (11) has a surface with substantially (100) orientation.

5. A process according to Claim 3, further comprising the step of performing chemical-etching of the surface of the Si substrate (11) using hydrofluoric acid to remove surface oxide film on the Si substrate;
   wherein said heat-heat treatment is performed in a mixture gas of arsine gas (AsH_3) and hydrogen and at a temperature of 900 ° C or higher.

6. A process according to Claim 5, wherein said heat-treatment is performed in a reduced-pressure MOCVD reactor in which the subsequent formation of the GaAs buffer layer (2) and the InP buffer layer (3) performed.

7. A process according to Claim 3, wherein said GaAs buffer layer (2) is formed to a thickness of about 20 nm (200 angstroms) or less by a reduced-pressure metal organic chemical vapor deposition using arsine gas and trimethylgallium (TMG) as raw materials and at a temperature of 450 ° C or lower (the lower limit is the limit of growth which is about 300 ° C).

8. A process according to Claim 3, wherein said InP buffer layer (3) is formed by a reduced-pressure metal organic chemical vapor deposition at a temperature of 550 ° C or lower, and using phosphine and trimethyl- indium (TMI) or triethyl-indium (TEI) as raw materials, with a molar ratio PH_3/TMI or TEI being in the order of 500.

9. A process according to Claim 8, wherein said reduced-pressure metal organic chemical vapor deposition is performed at a temperature not lower than about 300 ° C.

10. A process according to Claim 8, wherein the thickness of the InP buffer layer (3) is about 20 nm (200 angstroms).

11. A process according to Claim 3, wherein said InP monocrystalline thin film (4) is grown to a predetermined thickness, at a temperature of 600 to 650 ° C, using phosphine and TMI or TEI, as raw materials, with the molar ratio PH_3/TMI or TEI being about 100.

Patentansprüche

1. Halbleiter-Dünnschicht aus InP umfassend:
   ein Si-Substrat (1),
   eine auf dem Si-Substrat ausgebildete amorphe GaAs-Zwischenschicht (2),
   eine auf der GaAs-Zwischenschicht (2) ausgebildete amorphe InP-Zwischenschicht (3) und
   eine auf der InP-Zwischenschicht (3) ausgebildete, monokristalline InP-Dünnschicht (4).

2. Halbleiter-Dünnschicht gemäß Anspruch 1, wobei das Si-Substrat (1) eine Oberfläche mit einer im wesentlichen (100)-Orientierung aufweist.

3. Verfahren zur Herstellung einer Halbleiter-Dünnschicht aus InP, wobei das Verfahren die Schritte umfaßt:
Bereitstellen eines Si-Substrats (1),
Durchführen einer Wärmebehandlung des Si-Substrats (1),
Ausbilden einer amorphen GaAs-Zwischenschicht (2), die auf dem Si-Substrat (1) eine gute Oberflächenebenheit aufweist,
Ausbilden einer amorphen InP-Zwischenschicht (3), die auf der GaAs-Zwischenschicht eine gute Oberflächenebenheit aufweist und
Züchten einer monokristallinen Dünnschicht (4) auf der InP-Zwischenschicht (3).

4. Verfahren gemäß Anspruch 3, wobei das Si-Substrat (11) eine Oberfläche mit einer im wesentlichen (100)-Orientierung aufweist.

5. Verfahren gemäß Anspruch 3, das weiterhin den Schritt eines chemischen Ätzens der Oberfläche des Si-Substrats (11) unter Verwenden von Flußsäure zum Entfernen einer Oxydschicht auf der Oberfläche des Si-Substrats umfaßt,
wobei die Wärmebehandlung in einem Mischgas aus Arsingas (AsH_3) und Wasserstoff bei einer Temperatur von 900 °C oder höher durchgeführt wird.

6. Verfahren gemäß Anspruch 5, wobei die Wärmebehandlung in einem druckreduzierten MOCVD-Reaktor durchgeführt wird, in welchem die nachfolgende Ausbildung der GaAs-Zwischenschicht (2) und der InP-Zwischenschicht (3) durchgeführt wird.

7. Verfahren gemäß Anspruch 3, wobei die GaAs-Zwischenschicht (2) in einer Dicke von etwa 20 nm (200 Angström) oder weniger mittels einer druckreduzierten, metallorganischen chemischen Gasphasenabscheidung unter Verwenden von Arsingas und Trimetylgallium (TMG) als Ausgangssubstanzen und bei einer Temperatur von 450 °C oder weniger (die Untergrenze ist die Wachstumsgrenze bei etwa 300 °C) gebildet wird.

8. Verfahren gemäß Anspruch 3, wobei die InP-Zwischenschicht (3) mittels einer druckreduzierten, metallorganischen chemischen Gasphasenabscheidung bei einer Temperatur von 550 °C oder niedriger und unter Verwenden von Phosphin und Trimethylindium (TMI) oder Triethylindium (TEI) als Ausgangssubstanzen mit einem in der Größenordnung von 500 liegenden Molverhältnis für PH_3/TMI oder TEI gebildet wird.

9. Verfahren gemäß Anspruch 8, wobei die druckreduzierte, metallorganische chemische Gasphasenabscheidung bei einer Temperatur von nicht weniger als etwa 300 °C durchgeführt wird.

10. Verfahren gemäß Anspruch 8, wobei die Dicke der InP-Zwischenschicht (3) etwa 20 nm (200 Angström) ist.

11. Verfahren gemäß Anspruch 3, wobei die monokristalline InP-Dünnschicht (4) bis zu einer vorbestimmten Dicke bei einer Temperatur von 600 bis 650 °C unter Verwenden von Phosphin und TMI oder TEI als Ausgangssubstanzen mit einem Molverhältnis von etwa 100 für PH_3/TMI oder TEI gezüchtet wird.

Revendications

1. Film mince semi-conducteur en InP comportant :
un substrat Si (1);
une couche tampon de GaAs amorphe (2) formée sur le substrat Si;
une couche tampon d'InP amorphe (3) formée sur la couche tampon de GaAs (2); et
un film mince monocristallin en InP (4) formé sur la couche tampon d'InP (3).

2. Film mince semi-conducteur en InP selon la revendication 1, dans lequel ledit substrat Si (1) a une surface avec une orientation de sensiblement (100).

3. Procédé de fabrication d'un film mince semiconducteur en InP, ledit procédé comportant les étapes consistant à :
prévoir un substrat Si (1);
réaliser un traitement thermique du substrat Si (1);
former une couche tampon de GaAs amorphe (2) ayant une bonne planéité sur le substrat Si (1);
former une couche tampon d'InP amorphe (3) ayant une bonne planéité sur la couche tampon de GaAs; et
faire croître un film mince monocristallin en InP (4) sur la couche tampon d'InP (3).

4. Procédé selon la revendication 3, selon lequel ledit substrat Si (1) a une surface avec une

orientation de sensiblement (100).

5. Procédé selon la revendication 3, comportant en outre l'étape de réalisation d'une gravure chimique de la surface du substrat Si (1) en utilisant de l'acide hydrofluorique afin d'enlever le film d'oxyde de surface sur le substrat Si; ledit traitement thermique étant réalisé dans un mélange gazeux d'arsine (AsH_3) et d'hydrogène à une température de 900 °C ou plus.

6. Procédé selon la revendication 5, selon lequel ledit traitement thermique est réalisé dans un réacteur (MOCVD) à pression réduite dans lequel la formation consécutive de la couche tampon de GaAs (2) et de la couche tampon d'InP (3) est réalisée.

7. Procédé selon la revendication 3, dans lequel ladite couche tampon de GaAs (2) est réalisée avec une épaisseur d'environ 20 nanomètres (200 angstroems) ou moins par dépôt chimique en phase vapeur de métal organique à pression réduite en utilisant du gaz arsine et du triméthyl-gallium (TMG) comme matière de départ et a une température de 450 °C ou moins (la limite inférieure est la limite de croissance qui est d'environ 300 °C).

8. Procédé selon la revendication 3, dans lequel la couche tampon d'InP 3 peut être formé en utilisant un dépôt chimique en phase vapeur organique de métal à pression réduite à une température de 550 °C ou moins, et en utilisant de la phosphine et du triméthyl-indium (TMI) ou du triéthyl-indium (TEI) comme matières de départ, avec un rapport molaire PH_3/TMI ou TEI qui est de l'ordre de 500.

9. Procédé selon la revendication 8, dans lequel ledit dépôt chimique en phase vapeur organique de métal à pression réduite est réalisé à une température qui n'est pas inférieure à environ 300 °C.

10. Procédé selon la revendication 8, dans lequel l'épaisseur de la couche tampon d'InP (3) est d'environ 20 nanomètres (200 angstroems).

11. Procédé selon la revendication 3, dans lequel le film mince monocristallin en InP (4) est amené à croître à une épaisseur prédéterminée à une température de 600 à 650 °C en utilisant de la phosphine et du TMI ou du TEI comme matières de départ, avec le rapport molaire PH_3/TMI ou TEI d'environ 100.

FIG.1

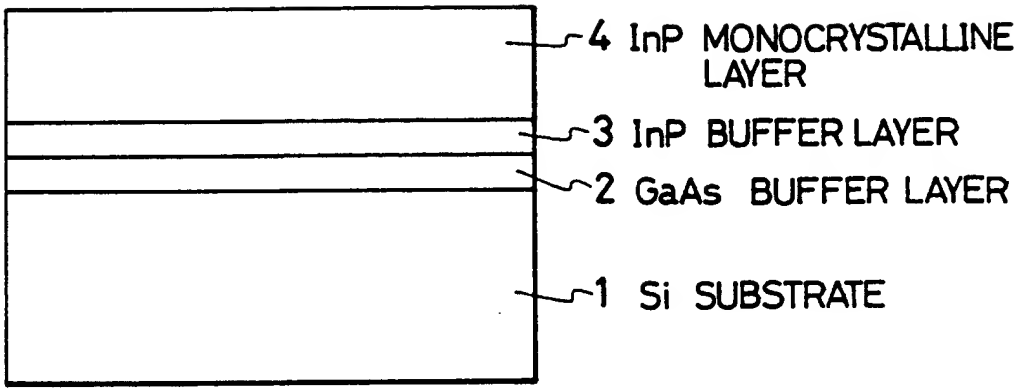

4 InP MONOCRYSTALLINE LAYER
3 InP BUFFER LAYER
2 GaAs BUFFER LAYER
1 Si SUBSTRATE

FIG.2

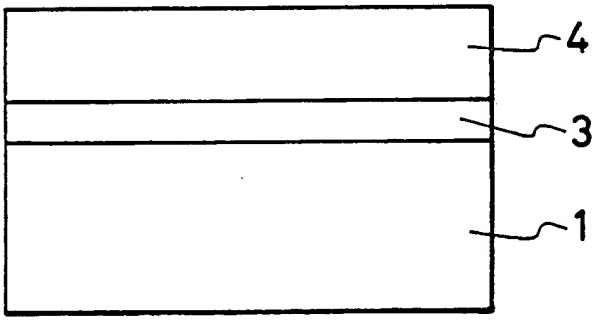
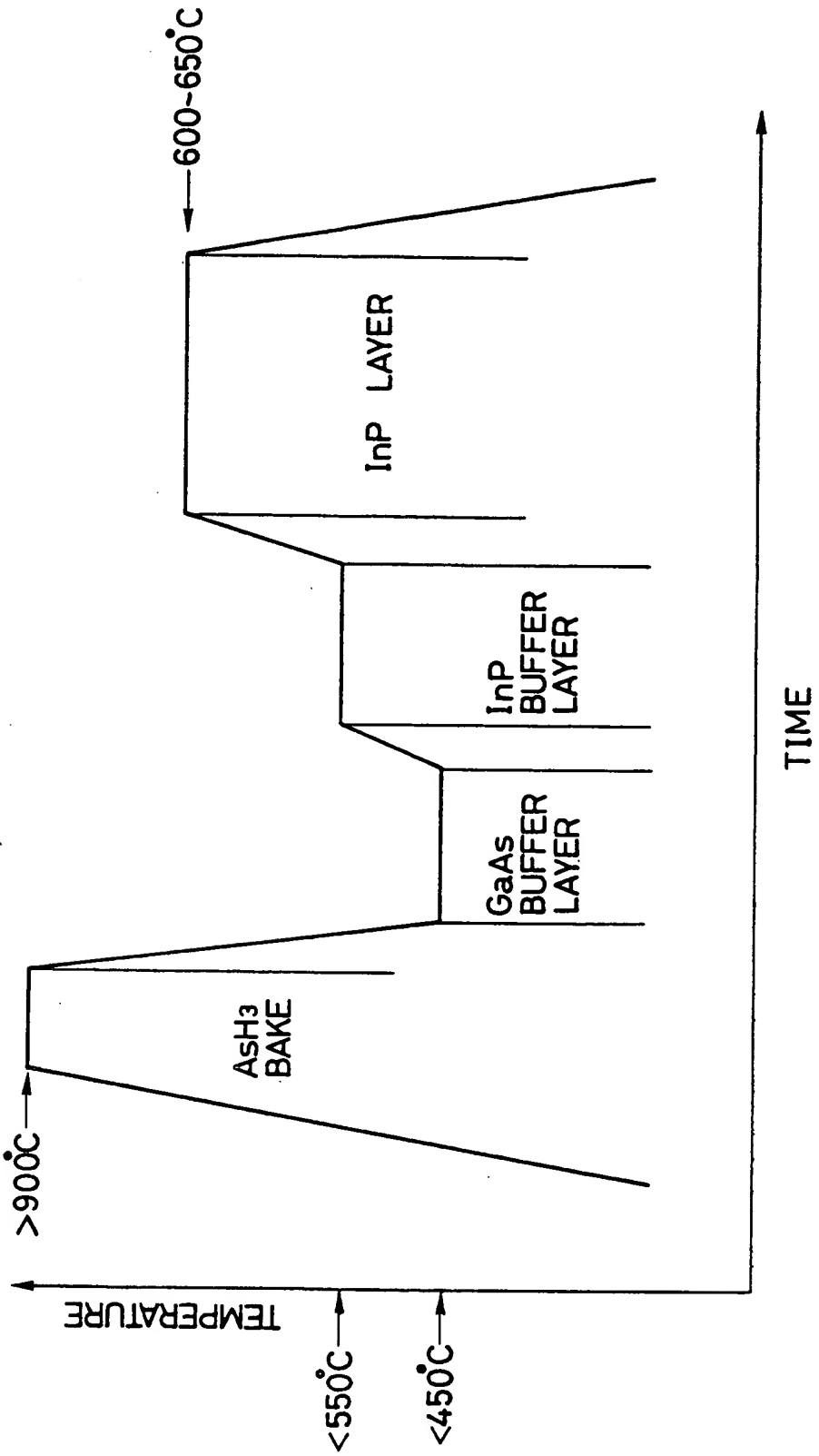

4
3
1

FIG.3


600-650°C
InP LAYER
InP BUFFER LAYER
GaAs BUFFER LAYER
AsH3 BAKE
>900°C
TEMPERATURE
<550°C
<450°C
TIME